REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have set forth the subject matter of previously considered claim 11, as new claim 34.

Moreover, Applicants have amended claim 19, in step (a), to recite a step of laminating "directly" to one side of a metal sheet an adhesive film for semiconductor use. Note, for example, Fig. 2, and the description in connection therewith on pages 40-42 of Applicants' specification. See also the first full paragraph on page 7 of Applicants' specification.

In addition to claim 34, Applicants are adding new claims 32 and 33 to the application. Claims 32 and 33, each dependent on claim 19, each further define the resin layer A, in terms of material thereof, consistent with the description on page 16 of Applicants' specification.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner in the statement of rejection, patentably distinguish over the teachings of the prior art applied by the Examiner in rejecting claims in the Office Action mailed May 15, 2007, that is, the teachings of the U.S. patents to Fjelstad, No. 6,856,235, to Lin, et al., No. 5,273,938, to Nishinaka, et al., No. 6,586,081, to Oka, et al., No. 6,132,865, and to Grupen-Shemansky, No. 5,268,065, under the provisions of 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method for producing a semiconductor device as in the present claims, having the steps (a)-(e) as set forth in claim 19, including wherein the adhesive film for semiconductor use is laminated directly to one side of a metal sheet, and wherein the method uses an adhesive film which comprises a support film and a resin layer A formed on one side or both sides

of the support film, the 90 degree peel strength between the resin layer A and the metal sheet (processed to give a wiring circuit), prior to the processing of the metal sheet, being 20N/m or greater at 25°C, and the 90 degree peel strengths, after molding, between the resin layer A and the wiring circuit and between the resin layer A and the molding compound both being 1000N/m or less at at least one point in the temperature range of 0°C to 250°C. Note claim 19.

As will be shown in the following, it is respectfully submitted that these applied references do not disclose, nor would have suggested, the use of the adhesive film in the process as in the present claims, wherein such adhesive film has the recited 90 degree peel strengths between the resin layer A of the adhesive film and various structures, during the process and advantages thereof.

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such method as in the present claims, having features as discussed previously in connection with claim 19, and, additionally (but not limited to), wherein the wiring circuit includes a plurality of patterns each having a die pad and an inner lead, and wherein the molded wiring circuit laminated with the adhesive film is divided to give a plurality of semiconductor devices each having one semiconductor die (see claim 20), in particular, wherein the step of electrically connecting the semiconductor die onto an exposed surface of the wiring circuit includes bonding the semiconductor die to the die pad and wire bonding the semiconductor die and the inner lead with wires (see claim 21).

Moreover, it is respectfully submitted that these applied references do not disclose, nor would have suggested, such method as in the present claims, having features of claim 19 as discussed previously, and, in addition (but not limited to), wherein the 90 degree peel strengths between the resin layer A and the wiring circuit

and between the resin layer A and the molding compound after molding are both 1000N/m or less at at least one point in the temperature range of 100°C-250°C (see claim 2); and/or further definition of the 90 degree peel strengths between the resin layer A and the wiring circuit and between the resin layer A and the molding compound, as in claims 3 and 29-31; and/or glass transition temperature of the resin layer A and temperature at which the resin layer A shows a 5wt% loss, as in claims 4 and 5, respectively, or elastic modulus of resin layer A as in claim 6; and/or specific materials of the resin layer A as in claims 7, 8, 32 and 33; and/or further definition of the 90 degree peel strength between the resin layer A and the metal sheet prior to the processing of the metal sheet, as in claims 23-25; and/or the 90 degree peel strength at 25°C between the resin layer A and the wiring circuit immediately before carrying out the molding step, as in claims 26 and 27; and/or wherein the step of peeling off the adhesive film is performed at a temperature in a range of 0°C to 250°C (see claim 22); and/or material of the support film of the adhesive film, as in claim 9; and/or ratio of thickness of the resin layer A to thickness of the support film, as in claim 10; and/or wherein the thickness of the adhesive film is 200µm or less (see claim 12); and/or the additional step of heating before the molding step, as in claim 28.

The Examiner is thanked for the indicated allowability of the subject matter of claim 11. In view thereof, claim 34, setting forth the subject matter of previously considered claim 11 in independent form, should be allowed.

The invention being considered on the merits in the above-identified application is directed to a method for producing a semiconductor device, including use of an adhesive film that enables a semiconductor package to be produced with high workability.

Recently, a method in which, after an adhesive tape is laminated to one side of a lead frame, a chip is mounted on the opposite side of the lead frame, and is wire bonded and molded, and subsequently the adhesive tape is peeled off, has been proposed. As described in the first full paragraph on page 2 of Applicants' specification, as another method for producing a semiconductor package, a method has been proposed in which, after a metal layer is formed on a temporary support substrate, a circuit is formed, and a chip is mounted, wire bonded, and molded, the temporary support substrate then being peeled off. However, it is not clear from this proposed method the necessary properties for the temporary support substrate.

Against this background, Applicants provide a method utilizing a specified adhesive film as a temporary support substrate, such that a resin molding compound utilized during a molding step is prevented from going around a wiring circuit of the device and the support substrate, and wherein glue residue is prevented from being present on the wiring circuit after peeling off of the support substrate. Applicants have found that by utilizing an adhesive film having a support film and a resin layer A formed on one or both sides of the support film, such resin layer A having specified 90 degree peel strengths at specific points in the manufacturing process with components adjacent thereto, the glue residue and undesirable passage of molding compound or other processing materials can be avoided. Specifically, by use of a 90 degree peel strength <u>between the metal sheet and the resin layer A</u> of at least 20N/m, circuit formation defects such as circuit erosion due to penetration of an etching solution during processing of the metal sheet can be avoided; and, moreover, even when the wiring circuit is narrow, peeling off of the adhesive film during a step in which the wiring circuit laminated with the adhesive film is washed or transported, can be avoided. Moreover, entry of molding resin between the wiring circuit and the resin layer A during the molding step can be avoided. Note the

paragraph bridging pages 8 and 9 of Applicants' specification, particularly page 9, lines 11-21.

In addition, by using an adhesion film having a 90 degree peel strength between the resin layer A and the wiring circuit immediately before carrying out the molding step as in various of the present claims, molding resin entering between the wiring circuit and the resin layer A during the molding step can be avoided. See the first full paragraph on page 10 of Applicants' specification.

Furthermore, by having a 90 degree peel strength between the resin layer A and the wiring circuit, and between the resin layer A and the molding compound, as in the present claims, stress on the wiring circuit or the molding compound, giving rise to the problem of breakage, can be avoided. Note the first full paragraph on page 12 of Applicants' specification.

In addition, with glass transition temperature (T_g), and 5% weight loss and elastic modulus at 230°C, as in various of the present claims, advantages are achieved as described on pages 14-16 of Applicants' specification.

As to advantages achieved by the present invention, attention is respectfully directed to Examples 1-12 on pages 40-52 of Applicants' specification, as compared with Comparative Examples 1-3 on pages 52-55 thereof. It is respectfully submitted that these examples constitute evidence that must be considered in any determination of obviousness. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984).

As stated in the last full paragraph on page 55 of Applicants' specification, it can be seen from the results of the Examples and Comparative Examples that the use of an adhesive film that has a 90 degree peel strength at 25°C of the resin layer A from a metal sheet, prior to processing of the metal sheet to give a wiring circuit, of 20N/m or greater; and 90 degree peel strengths between the resin layer A and the wiring circuit, and between the resin layer A and the molding compound, at at least

one point in the temperature range of 0°C-250°C after resin molding, of 1000N/m or less; and that can be peeled from the wiring circuit and the molding compound, can produce a semiconductor package with high workability and productivity without causing problems in any of the steps, including the metal sheet processing step.

In the Amendment filed February 16, 2007, Applicants relied on the evidence in their specification, as showing unexpectedly better results achieved by the present invention. However, the Examiner has not commented on such evidence, contrary to the guidelines of Manual of Patent Examining Procedure 716.01(a). It is respectfully submitted that the Examiner must consider evidence of record in the above-identified application; and, properly considered, it is respectfully submitted that such evidence establishes non-obviousness of the presently claimed subject matter.

Fjelstad discloses a resistor network having multiple different or common resistor values in a single device manufactured using a single sacrificial layer, and a method of forming such resistor network. Such method is described most generally in column 2, lines 2-25. This patent also provides a description of U.S. Patent No. 6,001,671 in, for example, from column 4, line 38 through column 9, line 45. As one alternative method of manufacture in No. 6,001,671, as described in Fjelstad, a sacrificial layer is comprised of a dielectric polymer sheet 100' having a conductive layer 101', typically a thin layer of copper, on one surface of the sacrificial layer 100' (note Figs. 2A-E). An array of conductive pads 110' are next photo-lithographically defined by etching away undesired sections of the conductive layer 101' so that the pads 110' define a central region 114' therebetween. Within the central region 114', a central conductive region 115' may also be defined by the pad-forming lithographic process; and a back surface 122' of a semiconductor chip 120' is then bonded to the conductive region 115' through the use of the thermally conductive die attached

adhesive 135'. Chip contacts on the exposed face surface 121' of the chip 120' are then electrically connected to respective pads 110' by wire bonding wires 130' therebetween; and the elements are next encapsulated using a suitable liquid encapsulate for the application and the encapsulate is cured. Portions of the polymer sheet 100' are then removed, as by chemically etching or laser ablation operations, so that the pads 110' and central conductive region 115' are exposed, and the packages may then be diced into either individual packages or multi chip packages. As another embodiment, this patent discloses a sacrificial layer comprised of a conductive metallic material, a polymer material or a combination of both a conductive metallic material and a polymer material.

It is respectfully submitted that Fjelstad would have neither disclosed nor would have suggested the presently claimed subject matter, including use of the adhesive film having the various 90 degree peel strengths, and advantages thereof. Noting especially that Fjelstad discloses chemical etching or laser ablation for removing portions of the polymer sheet, this patent would have taught away from the peel strength of the present claims, and advantages thereof, or the processing steps, including peeling off the adhesive film from the wiring circuit and molding compound.

Furthermore, Fjelstad would have neither disclosed nor would have suggested the other features of the present invention as discussed in the foregoing, and advantages thereof.

It is respectfully submitted that the additional teachings of the secondary applied references would not have rectified the deficiencies of Fjelstad, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Grupen-Shemansky discloses methods of thinning a semiconductor wafer, wherein a support film having a first major surface which has an adhesive strength of

less than approximately 20 grams per 25 millimeters of support film width at a 90° pulling angle, capable of withstanding temperatures up to approximately 200°C, is bonded to a first major surface of a semiconductor wafer. A desired thickness of a semiconductor wafer is removed from the second major surface. Subsequently, the support film is separated from the semiconductor wafer. Note column 2, lines 19-31. See also column 3, lines 7-9 and 21-28.

Oka, et al. discloses adhesive tapes for electronic parts to be used as adhesive tapes for fixing the lead frame , TAB tapes or for adhering between parts around lead frames making up a semiconductor device, the adhesive tape being described most generally from column 3, line 7 through column 5, line 53. Note also column 6, lines 27-37 and 50-58.

Nishinaka, et al. discloses polyimide/metal laminates wherein a polyimide film obtained by casting or applying a polyamic acid onto a substrate and dried to give a partly cured or partly dried film made of the polyamic acid or a polyimide, has applied thereto an organic solvent solution containing titanium element on the surface of the film, or has the film immersed in an organic solvent solution containing titanium element, the polyamide then being converted into the polyimide and the film then being dried. See column 2, lines 35-43. This patent discloses that the polyimide/metal laminate is one wherein the metal is laminated directly on the polyimide film by, for example, vacuum metallizing, sputtering or wet plating. See column 3, lines 31-34. This patent goes on to describe that the polyimide/metal laminate has an adhesive strength of 1,000N/m or more at pattern intervals of 3mm and at a peel angle of 90° and a peel speed of 50mm/min, and discloses that the metal is laminated on the polyimide film via an adhesive, for example, an epoxy adhesive, a nylon adhesive, an acrylic adhesive, an imide adhesive or a mixture of these adhesives. Note column 3, lines 44-52.

Note that Nishinaka, et al. discloses that the metal is laminated on the polyimide film via an adhesive. It is respectfully submitted that even assuming, arguendo, that the teachings of Nishinaka, et al. were properly combinable with the teachings of the other applied references, such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including wherein the adhesive film, comprising the resin layer A, is laminated directly to one side of the metal sheet. In this regard, it is respectfully submitted that the 90° peel strengths shown in Nishinaka, et al. represent peel strengths of the metal layers or the adhesives, not the adhesive strength of the polyimide film as contended by the Examiner. It is respectfully submitted that Nishinaka, et al. fails to disclose the adhesive strength of the polyimide film itself. It is respectfully submitted that the teachings of Nishinaka, et al., even as applied by the Examiner, and even in light of the teachings of the other references as applied by the Examiner, would have neither taught nor would have suggested the peel strength between the resin layer A and the metal sheet, in particular, 90° peel strength of 20N/m or greater at 25°C, or peel strengths between the resin layer A and wiring circuit and between the resin layer A and the molding compound, as in the present claims, and advantages thereof.

Lin, et al. discloses resin encapsulated semiconductor devices having multiple electronic components, and methods for fabricating such devices, wherein a semiconductor device is fabricated by providing a transfer film on which a pattern of conductive traces is provided. A first electronic component is interconnected to the pattern of conductive traces and a first package body is formed to encapsulate the first electronic component and first portion of the pattern of conductive traces. The transfer film is then removed to expose a second portion of the pattern of traces on a bottom surface of the first package body; and, thereafter, a second electronic

component is provided on the bottom surface of the first package body. A second package body is formed to encapsulate the second electronic component while leaving the second portion of the pattern of traces exposed. See column 2, lines 14-29. Note also the paragraph bridging columns 2 and 3; column 3, lines 25-27, 35-39 and 57-62; column 4, lines 9-13, 23-26, 34-36 and 4-46; and the paragraph bridging columns 4 and 5.

It is noted that Fjelstad discloses a method of making resistors, while Lin, et al. is directed to a method for attaching conductive traces to plural, stacked, encapsulated semiconductor dies. Fjelstad addresses the problem of reducing processing steps in making thick and thin film resistors, to provide resistor networks having multiple different or common values in a single device. In contrast, Lin, et al. is directed to overcoming problems in connection with previously proposed stacked devices, so as to avoid undesirable effects of the environment when providing stacked devices utilizing unpackaged dies. In view of differences between the technologies involved in connection with Fjelstad and Lin, et al., and differences in problems addressed, it is respectfully submitted that one of ordinary skill in the art concerned with in Fjelstad would not have looked to the teachings of Lin, et al. In other words, these references are directed to non-analogous arts.

Moreover, it is again emphasized that Lin, et al. is directed to providing stacked structures utilizing packaged dies so as to avoid undesirable effects of the environment, a problem different than that of the present invention. It is respectfully submitted that one of ordinary skill in the art concerned with in connection with the present invention would not have looked to the teachings of Lin, et al., to solve problems addressed therein; and, for this reason also, it is respectfully submitted that Lin, et al. constitutes non-analogous art.

In any event, advantages achieved by the present invention, having the peel strength prior to processing the metal sheet, and having the peel strengths in peeling off the adhesive film for semiconductor use after molding the semiconductor die and the exposed surface of the wiring circuit with a molding compound, are again noted. The applied references do not disclose, nor would have suggested, the better results achieved with such processing for forming the packaged semiconductor device as in the present claims. In light thereof, it is respectfully submitted that the presently claimed subject matter provides unexpectedly better advantages in view of the teachings of the applied prior art, establishing unobviousness of the presently claimed subject matter.

The interpretation by the Examiner of the teaching of Nishinaka, et al., on page 5 of the Office Action mailed May 15, 2007, is noted. As indicated previously, Nishinaka, et al. discloses peel strengths between the metal layer and adhesive, not between the metal layer and polyimide film. It is respectfully submitted that Nishinaka, et al. would have neither taught nor would have suggested the peel strength between the resin layer A and the metal sheet as in the present claims, and advantages thereof.

Reference by the Examiner to Fukumoto, et al., on pages 3 and 4 of the Office Action mailed May 15, 2007, is not understood. The Examiner has not applied Fukumoto, et al. in the statement of rejection; and, accordingly, application thereof is improper. See In re Hoch, 166 USPQ 406, 407 N.3 (CCPA 1970). Moreover, the Examiner has not discussed Grupen-Shemansky in the details of the rejection, although set forth in the statement of rejection.

In any event, Fukumoto, et al. discloses a surface protecting adhesive film for semiconductor wafers, to protect the surface thereof which makes it possible to straighten or avoid warpage of semiconductor wafers caused by the residual stress

of circuit protection films thereof. The adhesive film for protecting the surface of a semiconductor wafer, in Fukumoto, et al. is formed on one surface of a substrate film, the substrate film satisfying requirements as set forth in column 3, lines 18-33. Note also column 3, lines 34-49, for another embodiment of such adhesive film.

Even assuming, arguendo, that the teachings of Fukumoto, et al. were properly applied in the rejection, combination of the teachings thereof with the other applied references, even if properly combinable, would have neither taught nor would have suggested the laminating directly to one side of a metal sheet the adhesive film for semiconductor use, such adhesive film including the resin layer A having 90° peel strengths as in the present claims, the method including, inter alia, after processing the metal sheet to give a wiring circuit and electrically connecting a semiconductor die onto an exposed surface of the wiring circuit, molding the semiconductor die and exposed surface of the wiring circuit with a molding compound and peeling off the adhesive film from the wiring circuit and molding compound, with advantages achieved according to the present invention utilizing the adhesive film with peel strengths as in the present claims; and/or other features of the present invention as discussed previously, and advantages thereof.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants hereby petition for an extension of time under 37 CFR 1.136. Kindly charge any shortage of fees due in connection with the filing of this paper, including any extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (case 1204.44601X00), and please credit any overpayments to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By **/William I. Solomon/**
William I. Solomon
Registration No. 28,565

WIS/ksh
1300 N. 17th Street, Suite 1800
Arlington, Virginia 22209
Tel: 703-312-6600
Fax: 703-312-6666